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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,799	12/12/2003	Takashi Noma	492322015200	8803

25227 7590 06/09/2005

MORRISON & FOERSTER LLP
1650 TYSONS BOULEVARD
SUITE 300
MCLEAN, VA 22102

EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,799	NOMA, TAKASHI	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-10* is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 3 and 4 are rejected under 35 U. S. C. 102(b) as being anticipated by Applicant admitted Prior Art (AAPA) (See US 2004/0161920).

AAPA, in related text and figures (figs. 11, 13 and 14) discloses semiconductor device manufacturing method, comprising: providing a semiconductor wafer 124 provided with a plurality of metal portions 106 on a surface of the semiconductor wafer 124; suspending the semiconductor wafer 124 in a reflow furnace; reflowing the metal portions 106 on the surface of the semiconductor wafer 124 suspended in the reflow furnace so that the metal portions form conductive terminals using a first heater disposed in the reflow furnace and facing the surface of the semiconductor wafer **[0016]**.

2. Claims 1-4 are rejected under 35 U. S. C. 102(b) as being anticipated by Chroneos, Jr. et al. (US 6,805,279, herein after Chroneos, Jr.).

Chroneos, Jr., in related text and figures 5&6 discloses semiconductor device manufacturing method, comprising: providing a semiconductor wafer (circuit board) provided with a plurality of metal portions (solder balls) on a surface of the semiconductor wafer; suspending the semiconductor wafer in a reflow furnace; reflowing the metal portions on the surface of the semiconductor wafer suspended in the reflow furnace so that the metal portions form conductive terminals using a first heater disposed in the reflow furnace and facing the surface of the semiconductor wafer, wherein the semiconductor wafer is suspended by a plurality of pins (col. 5, lines 6-53).

3. Claims 1, 3 and 4 are rejected under 35 U. S. C. 102(e) as being anticipated by Lee et al. (US 6,805,279, herein after Lee).

Lee, in related text and figure 3 discloses semiconductor device manufacturing method, comprising: providing a semiconductor wafer 12 provided with a plurality of metal portions 26 on a surface of the semiconductor wafer 12; suspending the semiconductor wafer 12 in a reflow furnace (col. 8, lines 41-65); reflowing the metal portions 26 on the surface of the semiconductor wafer 12 suspended in the reflow furnace so that the metal portions 26 form conductive terminals 30 using a first heater disposed in the reflow furnace and facing the surface of the semiconductor wafer 12 (col. 9, lines 14-19).

Allowable Subject Matter

4. Claims 5-10 are allowed.

5. The following is an examiner's statement of reason for allowance: the prior art of record, either singularly or in combination, does not disclose or suggest that semiconductor device manufacturing method, comprising: supporting the semiconductor wafer using a plurality of pins that are in contact with the first supporting substrate; and reflowing the metal portions so as to from conductive terminals using a first heater disposed to face the back surface of the semiconductor wafer while the semiconductor wafer is supported by the pins, as instantly claimed and in combination with the additionally claimed method steps.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Vu

June 01, 2005.